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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,650	12/05/2003	Norihito Tsukahara	2003_1723A	8964

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EXAMINER	
NGUYEN, HOA CAO	
ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 05/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,650	TSUKAHARA ET AL.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) *16-39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1 PG*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 16-39 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention group, there being no allowable generic or linking claim. Applicant's election of group I, claims 1-15, in the reply filed on 4/4/06 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Claims 1-15 are treated on the merits in this Office Action.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Reference character 601, shown in figure 10, is not described in the specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims are rejected under 35 U.S.C. 102(b) as being anticipated by Ehman et al. (US 6021050).

Regarding claim 1, as shown in figures 1 and 2, Ehman et al. disclose a circuit board 10 (column 2, line 44), comprising:

(a) A base layer 14 (insulating layer, column 2, lines 45-49);

(b) a first conductive circuit 22/24 (pattern of electrical conductors, column 2, lines 60-63), manufactured by hardening a conductive paste material (screened-on or by any other conventional technique, column 1, lines 25-47 and column 2, lines 10-25) formed in a predetermined shape on the base layer;

(c) a first insulating layer 18 (intermediate layer, column 2, lines 54-56), manufactured by hardening an insulating paste material (epoxy resin for example, column 2, lines 22-25 and 46-54) formed on the base layer including the first conductive circuit; and

(d) a second conductive circuit 22/24 (same reference number, circuit patterns are formed on each layer, see column 2, lines 60-63), manufactured by hardening a conductive paste material formed in a predetermined shape on the first insulating layer

(screened-on or by any other conventional technique, column 1, lines 25-47 and column 2, lines 10-25).

Regarding claim 2, as shown in figure 1, Ehman et al. disclose the first insulating layer 18 is only on a part of the base layer 14. It is noticed that layer 14 contains areas for circuit patterns and electronic components; therefore insulating layer 18 is only on a part of the base layer.

Regarding claim 3, Ehman et al. disclose the base layer comprises a film member (any material - laminated of thin screened-on insulating layers, see column 2, line 46 and column 1, lines 25-47 - a thin screened-on insulating layer is considered as a film member).

Regarding claim 4, as shown in figure 1, Ehman et al. further disclose a plate member 20 (an intermediate insulating layer, column 2, line 55) on a part of a surface of the base layer that is opposite to surface of the base layer on which the first conductive circuit is formed (also see claim 2 above).

Regarding claim 5, Ehman et al. disclose the base layer comprises a plate member 20 (see claim 4 above).

Regarding claim 6, as shown in figure 1, Ehman et al. further disclose another plate member 12 (an insulating layer, column 2, line 45), wherein at least the first insulating layer 18 is positioned between the base layer and the another plate member.

Regarding claim 7, as shown in figure 1, Ehman et al. further disclose a connection opening 56 (holes, column 5, lines 43-51) in the first insulating layer on the

first conductive circuit, wherein the first conductive circuit and the second conductive circuit are electrically connected with each other via the connection opening.

Regarding claim 8, as shown in figure 1, Ehman et al. further disclose a resistance layer 26 (resistor, column 2, lines 63-66), formed by hardening a resistance paste material (resistive paste, column 3, lines 12-37) coated onto one of the base layer, wherein the resistance layer forms a resistor electrically connected to one of the first conductive circuit.

Regarding claim 9, as shown in figure 1, Ehman et al. further disclose a resistance layer 26 (resistor), formed by hardening a resistance paste material (resistive paste, column 3, lines 12-37) applied to a resistance opening (spaces for passive elements, column 2, lines 63-66) in the first insulating layer, wherein the resistance layer forms a resistor electrically connected to the first conductive circuit and the second conductive circuit (through conductive via 56). It is noticed that conductive vias 56 are for interconnection between circuit layers.

Regarding claim 10, as shown in figure 1, Ehman et al. further disclose a dielectric layer 48 (column 4, lines 32-61), formed by hardening a dielectric paste material (polymer dielectric ink) coated on the base layer, wherein the dielectric layer forms a capacitor 42 electrically connected to the first conductive circuit and the second conductive circuit.

Regarding claim 11, as shown in figure 1, Ehman et al. further disclose a dielectric layer 48 (column 4, lines 32-61), formed by hardening a dielectric paste material (polymer dielectric ink) applied to a dielectric opening (spaces for passive

elements, column 2, lines 63-66) in the first insulating layer, wherein the dielectric layer forms a capacitor 42 electrically connected to the first conductive circuit and the second conductive circuit.

Regarding claim 12, as shown in figure 1, Ehman et al. disclose a part of one of the first conductive circuit and the second conductive circuit forms an inductor 50 (column 5, lines 10-42).

Regarding claim 13, as shown in figures 2 and 3, Ehman et al. disclose the first conductive circuit and the second conductive circuit are connected to metallic wiring 22/24 (same reference number, copper, column 2, line 60 continuing column 3, line 11) formed by a conventional technique (also in column 2, lines 10-14), which inherently includes any one of a depositing, plating and sputtering process.

Regarding claim 14, as shown in figure 1, Ehman et al. disclose the metallic wiring is connected to an electrode terminal of bare chip IC 58/60 (other components, other electrical parts, column 5, lines 43-60). It is noticed that the term "other components/other electrical parts" includes bare chip/flip-chip, since bare chip is conventionally known in the art of printed circuit board and Ehman et al. does not have to disclose every details of connections outside the center of the invention (embedded passive components). Therefore, Ehman et al. anticipate the claim.

Regarding claim 15, Ehman et al. inherently disclose electronic parts mounted on the second conductive circuit, because Ehman et al. disclose a conventional multilayer circuit board and electronic parts mounted on a circuit layer or a wiring layer

are conventionally known in the art including surface mounting and embedded/buried electronic parts/components (see claim 14 above).

Citation of Relevant Art

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Liu et al. (US 20040037061) disclose a method and components for manufacturing multi-layer modular electrical circuits.

Hu (US 20040150966) discloses an integrated library core for embedded passive components and method for forming electronic device thereon.

Carpenter (US 6356455) discloses a thin integral resistor/capacitor/inductor package, method of manufacture.

Nakatani et al. (US 6734542) disclose Component built-in module and method for producing the same.

Bergstedt et al. (US 20030221864) disclose a printed board assembly and method of its manufacture.

Kimura et al. (US 6806428) disclose a module component and method of manufacturing the same.

Sugaya et al. (US 6538210) disclose a circuit component built-in module, radio device having the same, and method for producing the same.

Saia et al. (US 5874770) disclose a flexible interconnect film including resistor and capacitor layers.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen
4/26/06

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